Infineon Docket No. 2003P52595US
Attorney Docket No. INFN/0021
Express Mail No. EV335468450US

ECHO CLOCK ON MEMORY SYSTEM HAVING WAIT INFORMATION

ABSTRACT

A method and a circuit configuration for implementing a double data rate feature in a memory device capable of operating in a variable latency mode. The memory device may utilize a WAIT_DQS signal that combines functionality of a WAIT signal indicating when valid data is present on a data bus in Read cycle and the memory is ready to accept data in Write cycle, and a data strobe (DQS) signal.